SPECIFICATIONS

Model 2371 - Data Register

INPUTS (ECL, Z = 110 Ω)

Data: One 16-bit input on front-panel 34-pin header. Maximum rate 100 MHz.
Input Enable: One input via front-panel 2-pin header. Enables the Strobe signal. Minimum width 10 nsec. Unused input remains in the logical 1 state.
Strobe: One input on 2-pin header. Input data word is latched on leading edge of Strobe pulse. Minimum width 10 nsec.

OUTPUTS (ECL)

Data: Two 16-bit outputs on front-panel 34-pin headers. Input Data are latched into two output ports, compatible with ECLine data bus structure. Outputs are updated on receipt of an Input Strobe.
Data Ready: Two identical differential ECL outputs, each via a 2-pin connector on front panel. Output becomes valid 60 nsec +10% after the leading edge of the Input Strobe and remains valid until the leading edge of the next Input Strobe. Other delay times may be set via the Delay Adjustment potentiometer. See below.

GENERAL

Input-Output Delay: < 15 nsec from Input Strobe leading edge until front-panel output data is valid.
Delay Adjust: Board-mounted potentiometer. Used to set the delay between the Input Enable leading edge and the Output Ready leading edge. Factory set to 60 nsec +10%. Adjustable over the range 30-90 nsec.
Power: 300 mA at +6 V, 1.7 A at -6 V (12 W total).

Model 2373 - Memory Lookup Unit

INPUTS

Input Word: One 16-bit ECL input on front-panel 34-pin header with 100 Ω input impedance. Maximum rate: 22 MHz.
Enable: Four AND'd complimentary ECL pairs on front-panel header into 100 Ω impedance. Unused inputs are logically true. Required only in Strobe or Pulse Mode where Input Word is latched on leading edge of Enable pulse (coincidence of Enable Inputs being used).

OUTPUTS

Output Word: One 16-bit complimentary ECL output from a front-panel 34-pin header. In the Strobe or Pulse mode, the content of memory address given by the Input Word is presented 40 nsec after Input Enable. In the Transparent mode, the content of the addressed memory is presented 40 nsec after the Input Word.
Output Ready: Four complimentary ECL pairs from a front-panel header. Provides Output Ready level for down-stream logic indicating a valid Output Word.

OPERATING MODES

Operating modes are set by CAMAC commands.

TRANSPARENT: Latching is disabled. Output follows changing input with minimum propagation delay (40 nsec).
STROBE: Input Word latched on leading edge of AND of Input Enables. Ready appears 45 nsec after Enable.
PULSE: Same as Strobe Mode except that all true output bits go false after a delay which is adjustable (20-150 nsec) via a front-panel potentiometer. The purpose of this mode is to allow the scaling of individual bits of the Output Word.
INHIBIT: Disables front-panel inputs. Used for programming memory contents via computer.
Memory Configuration: Four 64K 4-bit Static RAMs make up the internal memory allowing 16-bit x 16-bit operation. It also can be configured to operate as a replacement for the Model 2373 with little or no programing changes required (see both Model 2373 and Model 2373 Owner's Manual). The memory in the Model 2373 has no battery back up like the Model 2372 and MUST be reloaded upon loss of power.
Computer Control: Read and Write Control Register (setting Mode and Dimensionality); Read and Write Address Register; Read or Write data at address in Address Register; Read front panel input word or the output generated by front-panel input.
PROPAGATION DELAY: In the Strobe and Pulse mode, propagation delay is defined as the time between the leading edge (trailing edge for "OR" condition) of the Input Enable signals at the front panel and the leading edge of the Output Ready signals. This is factory adjusted to 45 nsec. The Output Word settles at least 5 nsec before a true Ready condition, thus allowing for proper set up time at the inputs to successive stages of other LeCroy Programmable Data Handler Modules. In the Transparent mode, propagation delay is defined as the time between the leading edge of the Input Word at the front panel and the leading edge of the Output Word. This time is solely a function of the static RAM chips and is at most 40 nsec.

GENERAL

Maximum Rate: Transparent Mode to 25 MHz. All Other Modes to 22 MHz.
Power Requirements: +6 V at .7 A; -6 V at 2.3 A; -6 V (via Y1 pin) at .8 A. Note: -6 V is required on the Y1 pin to operate. (See CAMAC pin allocation specifications.)

Model 2375 - Data Stack

INPUTS (ECL, Z = 110 Ω)

Data Input: One 16-bit input on 34-pin header. Upper three bits may be used as steering bits, where the unit will only respond when these bits appear with programmed values. Maximum rate 20 MHz.

Memory Configuration: Internal memory is a 64K dual-ported RAM which is programmably configured to operate in one of 5 dimensionalities:

	Number of bits In	
Dimensionality	Input	Output
0	16	1
1	15	2
2	14	4
3	13	8
4	12	16

Battery backup of memory stores contents of memory and control registers during periods when power is off.

Computer Control: Read and Write Control Register (setting Mode and Dimensionality); Read and Write internal address register; Read or Write data at address in address register; Read front-panel input word or the output generated by front-panel input.

Power: +6 V/1.25 A, –6 V/850 mA (12.6 W Total).

MODEL 2375 DATA STACK (DS)

INPUTS (Front-panel, ECL,110 Ω impedance):

Data Input: One 16-bit input on 34-pin header. Upper three bits may be used for Steering Bits, where the unit will only respond when these bits appear with programmed values. Maximum rate 20 MHz.

Master Reset (MRST): One input on 2-pin header. Sets Read and Write Points to zero. Minimum width 10 nsec, reset time 30 nsec.

Write Enable (WE): Two bridged inputs on 2-pin header. Initiates writing DATA I to next memory location. If memory full, Write Overflow (WOF) is issued but pointer remains at end-of-memory.

All Data In (ADI): One input on 2-pin header. Sets the logical end-of-memory to the current WP. Read requests that access either the logical or physical end-of-memory result in resetting Read Pointer to zero, and continuing. If no ADI is issued and memory is not full, then read request awaits either another write or ADI.

Read Reset (RRST): One input on 2-pin header. Resets Read Pointer to zero. Minimum width 10 nsec, reset time 30 nsec.

Read Enable (RE): Two inputs on 2-pin header. On leading edge of RE, contents of memory at location given by Read Pointer (RP) are transferred to Data Output port, then RP is incremented by one. If operating results in RP>WP then a Read Overflow (ROF) is issued.

OUTPUTS (Front-panel, ECL):

Data Output (Data 0): One 16-bit output on 34-pin header. Memory contents addressed by Read operation presented at DATA 0.

Write Ready (WR): Two bridged outputs on 2-pin header. Indicate that a Write operation is complete.

Write Overflow (WOF): One output on 2-pin header. Indicates that 256 writes have been performed and memory is full.

Read Ready (RR): Two bridged outputs on 2-pin header. Indicates that output data word is ready to be read at DATA 0.

Read Overflow (ROF): One output on 2-pin header. Indicates that RP>WR. May be used to reset read pointer to zero by connecting to RRST.

Computer Control: Read and Write RP and WP; Read data word from memory addressed by RP; Write data word to address given by WP: MRST.

Power: +6 V/.25 A , –6 V/4.5 A (28.5 W Total).

MODEL 2376A DATA ARRAY (DA)

INPUTS (Front-panel Differential ECL, 110 Ω impedance):

Load Address (LA): One 13-bit input on 34-pin header. Lower 10 bits used for "hit" address and 3 bits used for steering bits: input steering bits are compared to side-panel switches, and the unit is activated only if they match.

Load Strobe (LSTB): One input via 2-pin header. If Load Strobe is Enabled and steering bits match switch settings, then the Load Address location is accessed and set to 1 regardless of previous input. Otherwise the Strobe is ignored. LSTB and SSTB must not occur simultaneously.

Load Strobe Enable (LSTE): One input via 2-pin header. Enables LSTB if ECL logical "1" or when disconnected.

Search Address (SA): One 13-bit input on 34-pin header accepts 10-bit address and 3-bit Search Width. If Search Strobe is Enabled then the addresses within ± search width of Search Address are examined for hit. If a hit is found, then the Status Bit output is set to 1.

Search Strobe (SSTB): One input via 2-pin header. If Search Strobe is Enabled then the addresses within ± search width of Search Address are examined for hit. Otherwise the search is ignored. SSTB and LSTB must not occur simultaneously.

Search Strobe Enable (SSTE): One input via a two-pin header. Enables Search Strobe if ECL logic "1" or input left unconnected.

All Data In (ADI): Input via two paralleled two-pin connectors suitable for Daisy-chaining. The rising edge of the ADI signifies that loading of addresses is complete and produces LC output. After ADI, the Load Strobe is disabled until the next MRST.

Master Reset (MRST): Input via two paralleled two-pin connector suitable for Daisy-chaining, resets memory, LAC, SAC, LC and STAT to "0". Minimum pulse width 50 nsec.

ECL OUTPUT (Front-panel, Differential ECL, 110 Ω impedance):

Status Bit (STAT): Output via a two-pin connector. Status Bit is true if at least one hit is present within the Search Width. Status Bit is reset by MRST, LSTB or CAMAC C, Z or F(9)A(0). It updates every time a Search Strobe is applied.

Status Bit Ready (SBR): Output via a two-pin connector. It goes to a logical "1" typically 60 nsec after the application of Search Strobe and indicates STAT is ready for reading.

Load Address Complete (LAC): Output via a two-pin connector to indicate the completion of a write operation. It goes to "0" at the application of Load Strobe (or MRST or SSTB), and goes to "1" typically 40 nsec later if Steering Bits match the switches.

Search Address Complete (SAC): Output via a two-pin connector to indicate the completion of a read operation. It goes to "0" at the application of Search Strobe (or MRST or LSTB), and goes to "1" typically 40 nsec later.

Loading Complete (LC): Output via a two-pin connector. Set to ECL logic "1" after ADI and reset to ECL "0" by MRST.

Computer Control: Write Address and either Search Width or Steering Bits: followed by either a LOAD or SEARCH command. Enable/disable Steering Bits, enable/disable wraparound (circular or linear mode), enable/disable front panel. Master Reset. Read address and Status Bit. Read Steering Bits and Steering Bit Switch settings.

Power: +6 V/2.2 A -6 V/2.2 A (26.4 W maximum).

MODEL 2378
ARITHMETIC LOGIC UNIT (ALU)

INPUTS (Front-panel, ECL, 110 Ω impedance):

Data (A and B): Two 16-bit inputs on 34-pin header. Input A used for two input word operations only, input B used for all operations. Input A switchable to output C for accumulator mode.

Strobe (A and B): Two, each on 2-pin header, internally AND'd with unused input held logically true. Leading edge latches Data input. Strobe ignored if corresponding input not used. Maximum rate 20 MHz.

Carry: One, on 2-pin header. Accepts carry bit from second ALU for 32-bit arithmetic operations. Ignored on logical operations.

Op-Code: One, 4-bit input on multi-pin header. Desired ALU operation set by one of 16 combinations presented.

Op-Code Strobe: One, on 2-pin header. Op-code latched on leading edge of strobe. Input Data strobe must be delayed by at least 20 nsec after op-code strobe. Maximum rate 20 MHz.

Clear (A and B): One each on 2-pin header. Each clears input register independently.

OUTPUTS (Front-panel, ECL):

Data (C): One, 16-bit output on 34-pin header. Contains result of ALU operation.

Data Ready: One, on 2-pin header. Gives 20 nsec long pulse when Data C bits are valid.

Carry: One, on 2-pin header. Provides carry bit for use as overflow or for 32-bit operation by connection to carry-in bits of another ALU module.

Operations:

C = previous C + B	C = A + B	C = 2 A
C = previous C - B	C = A - B	C = A - 1
C = A	C = B	C = (0000)hex
C = A AND B	C = A or B	C = (1111)hex

C = A XOR B (Logical operations are bit-wise combinations. Some operations differ only in that one strobe latches both inputs, bringing the total number of op-codes to 16.)

Computer Control: Clear registers A and B, enable/disable front panel, read latched op-code, read output C, write op-code, generate Strobes A and B.

Power: +6 V/.6 A, -6 V/3.3 A (23.4 W Total).

Packaging for the above modules: In conformance with CAMAC standard for nuclear modules (ESONE Committee Report EUR4100 or IEEE Report 583). RF-shielded CAMAC #1 module.

3A

CAMAC FUNCTION CODES, COMMANDS and RESPONSES

MODEL 2371 DATA REGISTER

N•F(0)•A(0)	Read 16-bit word.
X:	An X=1 response is generated for any valid CAMAC command.

MODEL 2372 MEMORY LOOKUP UNIT

F(0)•A(0)	Read 1 to 16-bit Output word addressed by CAMAC Address Register (CAR). Increment CAR. Requires operation in Inhibit mode. Inactive bits are not masked and are arbitrary.